

Table 1: LV_CHAN State Transition Table:

		Final State			
		Stopped	LV_OFF	LV_ON	LV_VCSEL
Initial State	Stopped	/	Start(i) && !SWIL(i) && !DCSIL /	/	/
		ChStat(i).Hwon=0 ChStat(i).Swon=0	ChStat(i).Hwon=1 ChStat(i).Swon=0	/	/
	LV_OFF	Stop(i) Ttrip(i) Crow(i) SWtrip(i) SWIL(i) DCSIL /	ChStat(i).Hwon=1 ChStat(i).Swon=0	SwitchOn(i) && !VCSELIL /	SwitchOn(i) && VCSELIL /
		ChStat(i).Hwon=0 ChStat(i).Swon=0		ChStat(i).Hwon=1 ChStat(i).Swon=1	ChStat(i).Hwon=1 ChStat(i).Swon=1
LV_ON	Stop(i) Ttrip(i) Crow(i) SWtrip(i) DCSIL SWIL(i) /	SwitchOff(i) Ctrip(i) /	!VCSELIL /	VCSELIL /	
	ChStat(i).Hwon=0 ChStat(i).Swon=0	ChStat(i).Hwon=1 ChStat(i).Swon=0	ChStat(i).Hwon=1 ChStat(i).Swon=1	ChStat(i).Hwon=1 ChStat(i).Swon=1	
LV_VCSEL	Stop(i) Ttrip(i) Crow(i) SWtrip(i) SWIL(i) DCSIL /	SwitchOff(i) Ctrip(i) /	!VCSELIL /	VCSELIL /	
	ChStat(i).Hwon=0 ChStat(i).Swon=0	ChStat(i).Hwon=1 ChStat(i).Swon=0	ChStat(i).Hwon=1 ChStat(i).Swon=1	ChStat(i).Hwon=1 ChStat(i).Swon=1	

Notes:

Definitions;

These definitions refer to Jan Stastny's documents on the SCT LV power supply [1], [2].

LV_CHAN[i] LV channel for module i, where i = 0:3.
LV_CARD One LV card with 4 LV_CHANs

Serial Command Data:

BdStat board status byte.
BdStat.VCI VCSel Interlock bit.
BdSet Board setting sequence.
ChMask Channel Mask byte. Range = 0x00 (all on) to 0x0F (all off).
ChStat(i) Channel status byte for channel i, where i = 0:3.
ChSet(i) Channel setting sequence for channel i.
ChCtrl(i,R,S,On) Channel control byte for channel i. R = Reset; S = Select; On = On/Off.
ChCtrl(3,0,0,1) Means switch on channel 3 without resetting it.
ChMon(i) Channel monitoring sequence for channel i.

Commands from DCS to LV_CARD:

Start(i) Start channel i: Send ChSet(i) with ChMask bit[i]==0.
Stop(i) Stop channel i: Send ChSet(i) with ChMask bit[i]==1.
SwitchOn(i) Switch on channel i: Send ChSet(i) with ChCtrl(i,1,0,0)
 then send ChSet(i) with ChCtrl(i,0,0,1).(?)
SwitchOff(i) Switch off channel i: Send ChSet(i) with ChCtrl(i,0,0,0).

Events:

Ctrip(i) Current trip in channel i.
Crow(i) Crowbar (overvolts) trip in channel i.
SWtrip(i) Software trip in channel i (= communication error).
Trip(i) Module temperature trip in channel i.

Interlock Conditions:

DCSIL DCS interlock (stops all 4 channels).
SWIL(i) Software interlock on channel i.
VCSELIL VCSEL interlock (switches off VCSELS for whole crate).

Table 2: Module State Transition Table

Final State

		Final State			
		MODLV_OFF	MODLV_ON	Configured	Sensitive
Initial State	MODLV_OFF	!LV_ON /	LV_ON /		
	MODLV_ON	!LV_ON /	LV_ON /	LV_ON && !HV_ON && Config() /	LV_ON && HV_ON && Config() /
	Configured	LV_OFF LV Stopped /	DAQ error? /	(LV_ON && !HV_ON) LVVCSSEL /	LV_ON && HV_ON /
	Sensitive	LV_OFF LV Stopped /	DAQ error? /	(LV_ON && !HV_ON) LVVCSSEL /	LV_ON && HV_ON /