

PHOS4 Anomalous Behaviour

Outline

It has been known that some PHOS4s can lock into an anomalous state, but it had until recently only been clearly identified on rare occasions during Mustard commissioning. Enhancements of the Mustard test software and the chance happening upon a bad set of PHOS4 chips have given new insight into the condition. The problem is that the PHOS4 is designed to adjust the speed of a chain of 25 buffers to give a delay that is an integral number of clock periods. This should be one period, but it seems that on occasions it attempts to reach the neighbouring solutions of 0 or 2 periods. Obviously 0 is not achievable, and it appears that 2 isn't either; but the loop locks at the minimum or maximum delay limits. This means that the chip then no longer delivers delay steps of 1ns, but around 0.6ns in the 'FAST' state, or around 1.8ns in the 'SLOW' state. Note that we are not yet able to assess what proportion of PHOS4 chips exhibit this anomalous behaviour during normal use. The evidence for these mal-functions is given later.

Implications for Mustard

Arguably this is not a major problem for Mustard, since it has been in wide use without serious difficulties. The commissioning procedure used to date showed up the 'bad offenders', and the PHOS4s were replaced. Usually power cycling the module causes the problem to go away. It would obviously be desirable to be able to offer a fix for the problem.

Implications for BOC

These are far more serious, both in that BOC is to be used for real data in a complex system, and because each BOC uses 26 PHOS4 chips. Power cycling is not an acceptable fix. Even if it were, it is unlikely to leave all 26 in the correct state. What is needed is a 'corrective procedure' that forces all the PHOS4s out of these anomalous states.

What to do about it

We have been following a 3 pronged attack on the problem:

1. Understanding PHOS4 behaviour:
 - What gets them into such states
 - What proportion of them are liable to fail in these ways
 - What 'Corrective Action' can be taken to get them out of these states
2. BOC Modifications to allow the operation of the PHOS4s to be checked
3. BOC (and Mustard) Modifications to incorporate 'Corrective Action'

How it Shows up

Mustard uses its PHOS4 delay chips to delay the 12 data streams so the strobing into the data registers occurs when the data is stable. The Mustard test procedure uses SLOG to provide 12 streams of valid data with little skew between the streams. The data delays are scanned through the settings 0-24. The data is registered before entering the Stream FIFOs. The Event Builder takes the data from the FIFOs and

makes the events it builds available via the VME; it counts errors in the data structure as it does this. The test program records how this error rate varies with delay setting: the latest version does this on a per-stream basis. Fig 1 shows the results when the PHOS4s are working correctly. We have found a set of 3 PHOS4s that seem particularly susceptible to anomalous behaviour: the other figures show various combinations of SLOW and FAST operation that have been seen. SLOWness gives 2 peaks in the delay scan. These are seen to be 14 steps apart, and must correspond to 25ns change in delay: a step size of 1.8ns: oscilloscope measurements confirm this interpretation. FASTness gives a single, broadened peak that occurs at roughly twice the delay setting. We can't precisely infer the delay-per-step from this, since there is a non-zero delay through the PHOS4s at zero setting. Scope observations indicate that the delay-per-step is around 0.6ns.

PHOS4 Investigations

A BOC1 board has been used in bench tests to look at how PHOS4s behave in BOCs. One of the PHOS4 sites has been equipped with a PLCC socket to facilitate the swapping of chips. The ability to drive the PHOS4 clock from a signal generator and to feed a test signal into one of the PHOS4 slave delay streams have been patched in.

Using this set-up, the range over which the PHOS4 will hold correct lock as the input frequency is varied has been explored. The phase comparator output has been observed during such manipulations (this can be selected as the PHI 2 clock output using delay setting 26).

- SLOW operation has been seen with both the 'susceptible' and a couple of non-selected PHOS4s: it can be reliably induced by removing the clock feed to the PHI 1 pin of the PHOS4.
- The PHOS4 can be pulled out of SLOW operation by reducing the clock frequency to 10 MHz for a short time: this offers hope as a corrective action.
- FAST operation has not been seen with this set-up.

Corrective Action

Tests are being pursued using a Mustard with the 3 'susceptible' PHOS4s. The firmware in the Mustard Input Controller CPLD (IPCont) has been modified to allow the PHOS4 clock to be manipulated. It can be divided down to 20 or 10 MHz, or turned off under VME control. So far this work confirms that:

- Power Cycling can yield NORMAL, FAST or SLOW operation, or a mix of FAST and NORMAL, or of SLOW and NORMAL. We have not seen a mix of FAST and SLOW mode PHOS4s.
- SLOW PHOS4s can be forced into NORMAL operation by interrupting the clock (i.e. Forcing it to 0) for 100ms (this seems to work at least 90% of the time).

The first indications are that FAST operation is not cured by a burst of 10 MHz clock, but this work needs to be confirmed.

Planned Changes to BOC

Small additions to BOC circuitry should allow the performance of all the PHOS4s to be checked. This would imply some changes to the Address Map (the addition of a new Control Register, and pushing the hitherto unused 'Clock Delay' streams of the PHOS4s into service). That means some 27 extra addresses that were previously unused. It

would also call upon ROD to support for some additional delay scans: these would be very similar to those already required for other BOC timing operations.

Hopefully Corrective Actions can be found that can be incorporated within the control CPLD and clock generation circuits without serious changes to the hardware.

Conclusions

These investigations are clearly very important, and are continuing.

...ooOoo...

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22-Jul-02 A035 Delay Data Scan showing all PHOS4s working correctly
Del Stream
Val << ----- >>
=== 1 2 4 Enables ----- >>
0 . . 15 8 10 20 40 80 100 200 400 800 fff
1 . . . . . . . . . . . . . .
2 . . . . . . . . . . . . . .
3 . . . . . . . . . . . . . .
4 . . . . . . . . . . . . . .
5 . . . . . . . . . . . . . .
6 . . . . . . . . . . . . . .
7 . . . . . 2777 . . . . . . . .
8 3987 3971 . 3940 2737 3985 1611 2781 3985 3986 2096 11 2507
9 2709 3998 3986 3999 17 2287 3992 3934 2663 2675 3991 3986 3999
10 18 39 2668 41 . 3 39 29 7 6 40 40 570
11 . . 16 . . . . . . . . . . . .
12 . . . . . . . . . . . . . .
13 . . . . . . . . . . . . . .
14 . . . . . . . . . . . . . .
15 . . . . . . . . . . . . . .
16 . . . . . . . . . . . . . .
17 . . . . . . . . . . . . . .
18 . . . . . . . . . . . . . .
19 . . . . . . . . . . . . . .
20 . . . . . . . . . . . . . .
21 . . . . . . . . . . . . . .
22 . . . . . . . . . . . . . .
23 . . . . . . . . . . . . . .
24 . . . . . . . . . . . . . .
    
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Fig 1: All PHOS4s Normal

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16-Jul-02 A035 showing all PHOS4s slow
Val << ----- >>
=== 1 2 4 Enables ----- >>
0 1 . . . 8 10 20 40 80 100 200 400 800 fff
1 1 . . . . 1 . . . . 1 . . . .
2 . . . . . . . . . . . . . .
3 . . . . . . . . . . . . . .
4 790 . . . . 985 702 . . . . 28 . . . . 999
5 30 306 986 641 42 10 326 622 1 1 599 638 999
6 . . 41 16 . . . . 2 14 . . . . 14 . .
7 . . . . . . . . . . . . . .
8 . . . . . . . . . . . . . .
9 . . . . . . . . . . . . . .
10 . . . . . . . . . . . . . .
11 . . . . . . . . . . . . . .
12 . . . . . . . . . . . . . .
13 . . . . . . . . . . . . . .
14 . . . . . . . . . . . . . .
15 . . . . . . . . . . . . . .
16 . . . . . . . . . . . . . .
17 . . . . . . . . . . . . . .
18 938 . . . . 985 630 . . . . 727 631 . . . . 999
19 37 634 985 700 42 14 639 645 35 16 112 608 999
20 . 12 41 5 . . . . 18 10 . . . . 13 . .
21 . . . . . . . . . . . . . .
22 . . . . . . . . . . . . . .
23 . . . . . . . . . . . . . .
24 . . . . . . . . . . . . . .
    
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Fig 2: All PHOS4s Slow

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After Clock interruption:
Val << ----- >>
=== 1 2 4 Enables ----- >>
0 1 . . . . 1 . . . . 1 . . . .
1 . . . . . . . . . . . . . .
2 . . . . . . . . . . . . . .
3 . . . . . . . . . . . . . .
4 . . . . . . . . . . . . . .
5 . . . . . . . . . . . . . .
6 . . . . . . . . . . . . . .
7 . . . . . . . . . . . . . .
8 . . . . . 986 985 . . . . 344 2 . . . . 999
9 . . . . . 39 981 985 985 992 985 985 985 999
10 . . . . . . 34 40 39 42 40 39 84 21
11 . . . . . . . . . . . . . .
12 . . . . . . . . . . . . . .
13 . . . . . . . . . . . . . .
14 4 . . . . . . . . . . . . . . 738
15 987 126 . . . . . . . . . . . . . . 999
16 999 988 . 986 . . . . . . . . . . 999
17 645 999 985 999 . . . . . . . . . . 999
18 12 49 999 537 . . . . . . . . . . 999
19 . . . 796 10 . . . . . . . . . .
20 . . . 13 . . . . . . . . . .
21 . . . . . . . . . . . . . .
22 . . . . . . . . . . . . . .
23 . . . . . . . . . . . . . .
24 . . . . . . . . . . . . . .
    
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Fig 3: First PHOS4 Fast, others Normal

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After Clock interruption:
Del
Val << ----- >>
=== 1 2 4      Stream
      . . .      Enables ----- >>
0    1 . . .      8 10 20 40 80 100 200 400 800 fff
1    . . .      . . . . .
2    . . .      . . . . .
3    . . .      . . . . .
4    854 . . .    . . . . .
5    34 214 985 674 . . . . .
6    . 4 42 10 . . . . .
7    . . .      . . . . .
8    . . .      . 985 986 . . . 489 15 . . . 999
9    . . .      . 39 872 986 986 994 986 986 985 999
10   . . .      . . 18 41 40 39 39 41 61 21
11   . . .      . . . . .
12   . . .      . . . . .
13   . . .      . . . . .
14   . . .      . . . . .
15   . . .      . . . . .
16   . . .      . . . . .
17   . . .      . . . . .
18   981 . . .    . . . . .
19   34 627 985 678 . . . . .
20   . 13 40 6 . . . . .
21   . . .      . . . . .
22   . . .      . . . . .
23   . . .      . . . . .
24   . . .      . . . . .
    
```

Fig 4: First PHOS4 Slow, others Normal

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After Clock interruption:
Del
Val << ----- >>
=== 1 2 4      Stream
      . . .      Enables ----- >>
0    1 . . .      8 10 20 40 80 100 200 400 800 fff
1    . . .      . . . . .
2    . . .      . . . . .
3    . . .      . . . . .
4    179 . . .    . 985 690 . . . . . 999
5    3 678 985 927 39 13 281 636 . . . . . 999
6    . 16 39 28 . . . 5 22 . . . . .
7    . . .      . . . . .
8    . . .      . . . . . 440 5 . . . 996
9    . . .      . . . . . 987 986 985 986 999
10   . . .      . . . . . 39 42 40 71 21
11   . . .      . . . . .
12   . . .      . . . . .
13   . . .      . . . . .
14   . . .      . . . . .
15   . . .      . . . . .
16   . . .      . . . . .
17   . . .      . . . . .
18   165 . . .    . 985 646 . . . . . 999
19   363 794 985 976 40 15 653 656 . . . . . 999
20   . 5 40 38 . . . 12 14 . . . . .
21   . . .      . . . . .
22   . . .      . . . . .
23   . . .      . . . . .
24   . . .      . . . . .
    
```

Fig 5: First 2 PHOS4s Slow, third Normal

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After Power Cycle:
Del
Val << ----- >>
=== 1 2 4      Stream
      . . .      Enables ----- >>
0    . . .      1 1 . 1 1 . . . . .
1    . . .      . . . . .
2    . . .      . . . . .
3    . . .      . . . . .
4    . . .      . . . . .
5    . . .      . . . . .
6    . . .      . . . . .
7    . . .      . . . . .
8    . . .      . 985 987 . . . 626 67 . . . 999
9    . . .      . 34 740 986 985 993 987 985 986 999
10   . . .      . . 15 39 39 39 39 82 524 18
11   . . .      . . . . . . . 2 13 . . .
12   . . .      . . . . .
13   . . .      . . . . .
14   152 . . .    . . . . . . . . . 677
15   991 235 . .    10 . . . . . . . . . 999
16   999 988 73 986 . . . . . . . . . 999
17   657 999 985 999 . . . . . . . . . 999
18   18 40 999 682 . . . . . . . . . 999
19   . . . 684 12 . . . . . . . . . 325
20   . . . 15 . . . . . . . . . . .
21   . . .      . . . . .
22   . . .      . . . . .
23   . . .      . . . . .
24   . . .      . . . . .
    
```

Fig 6: First PHOS4 Fast, others Normal

